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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,053	08/18/2001	Chi Chuan Wu	56386	5051

21874 7590 10/28/2003

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/932,053	WU ET AL.	
	Examin r	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication app ars on the cover sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Remarks

1. Applicant's RCE filling request is acknowledged.

2. Claims 1-20 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 7, 10-15, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs et al.(US 5,355,283) in view of Richman (US 5,249,354).

Marrs et al. teach the claimed method and semiconductor package, comprising:

- providing a substrate 602 having a device-mounting region, i.e. the region for passive devices (col. 2, lines 66-67), predefined with a chip-mounting region on a surface of the substrate (Fig.6), and a wire bonding region, i.e. the region where traces 605 are located, predefined around the device-mounting region;
- mounting a plurality of passive devices on the device-mounting region (col. 2, lines 66-67, wherein Marrs et al. suggest that passive components can be mounted on the substrate);
- after mounting the passive devices using an insulative material 609 for encapsulating the passive devices (col. 3, lines 20-21; col. 8, lines 27-35), wherein the insulative material may be thermosetting or thermoplastic (col.7, lines 26-30);

- disposing a semiconductor chip 601 on a surface of the insulative material above the passive devices, such that the semiconductor chip 601 is free of contact with the passive devices (not shown) and the substrate 602 because a protruding portion of the insulating material 609 over a central region of the substrate 602 physically separates the semiconductor chip 601 from the substrate 602 on which has passive components form; and wherein the chip 601 has an active surface (a top surface) and an inactive surface (a bottom surface) (Fig.6);
- providing a plurality of bonding wires 606 for electrically connecting the semiconductor chip 601 to the traces 605 (Fig.6);
- forming an encapsulant 603 for encapsulating the semiconductor chip 601 and the bonding wires 606 (Fig.6); and
- providing a plurality of conductive members 604 for electrically connecting the substrate 602 to an external device (Fig.6).

Marrs et al. do not teach utilizing the bonding wires 606 for electrically connecting the semiconductor chip 601 to the bonding fingers of the substrate.

However, Richman in an analogous art of making a semiconductor package teaches making the package 20 (Fig.2) containing a chip 25 and/or other passive components (see abstract); providing a plurality of bonding wires 23 for electrically connecting the chip 25 to bonding fingers 21; and forming an encapsulant 24 for encapsulating the chip 25 and the bonding wire 23.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the chip of Marrs et al. to the bonding finger as taught by

Richman since by this manner it would provide a physical support during the fabrication of the package (col. 3, lines 50-61).

5. Claims 6, 8, 9, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs and Richman as applied to claims 1, 7, 11 and 17 above and further in view of Falcone et al. (US 6,022,583).

Marrs in view of Richman fails to teach encapsulating the passive devices through a dispensing process. However, utilizing the dispensing process for encapsulation in packaging applications is a well-known technique, as evidenced by Falcone et al. (col. 2, lines 14-30).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the dispensing process of Falcone et al. in the packing method of Marrs in view of Richman for encapsulating the top surface and periphery of the passive devices and attaching the inactive surface (the bottom surface) of the chip directly to the surface of the insulative material above the passive devices before the insulative material is cured since by this manner it would form a good encapsulation to enclose the packaging without the formation of voids.

Response to Arguments

6. Applicants' arguments filed 7/14/03 have been fully considered but found not persuasive for reasons as follow.

Applicants' arguments are on the ground that Marrs et al. fail to teach or suggest positioning the semiconductor chip above the pre-encapsulated passive components and free of contact with the passive devices and substrate (second paragraph, page 2 of REMARKS).

Contrary to the argument, Marrs et al., in col.2, lines 66-67, clearly indicate that passive components, such as resistors and capacitors, can also be mounted on the substrate. After mounting the passive components on the substrate, the insulating material 609 is covered on the substrate 602 followed by mounting the semiconductor chip 601 thereon. In other words, Marrs et al. teach that the insulating material 609 (i.e. the protruding portion of the insulating material 609 over a central region of the substrate 602) physically separates the semiconductor chip 601 from the passive components and the substrate 602. Thus, the semiconductor chip 601 does not contact with the passive devices and the substrate.

Applicant also argues that "[I]t is apparent from Marrs that, if passive components are included in a package, they would be mounted on a substrate beside the semiconductor chip. (first paragraph, last page).

In response to the above argument, the applicant is invited to specifically point out where the teaching is. It is the Examiner's position that the above argument is based on applicant's assumption, not factual evidence from Marrs reference.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP 11-260999 teaches a relative art (i.e. BGA), in which passive component are arranged in laminated type, i.e. the passive components are placed on the semiconductor substrate, not beside the semiconductor chip. By this arrangement, it would improve package density of the semiconductor device.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

Oct. 17,2003